

ABSTRACT OF THE DISCLOSURE

A circuit and method are described in which a DC voltage or current is connected to a high frequency, AC-coupled signal path between a transmitter and a receiver, and the bit error rate of the data transmission is tested while applying an altered bias voltage to the received signal. The bias voltage can be connected via a resistor, inductor or transistors. The transmitted signal is attenuated resistively, and a load capacitance is applied whose value causes digital transition times to exceed one unit interval. An intended application is testing of an integrated circuit, serializer/deserializer (serdes) operating above 1 GHz.